

# WP4 Safety and security

## WP4T43-06: FPGA Fault Injection Tool (DAVOS FFI)

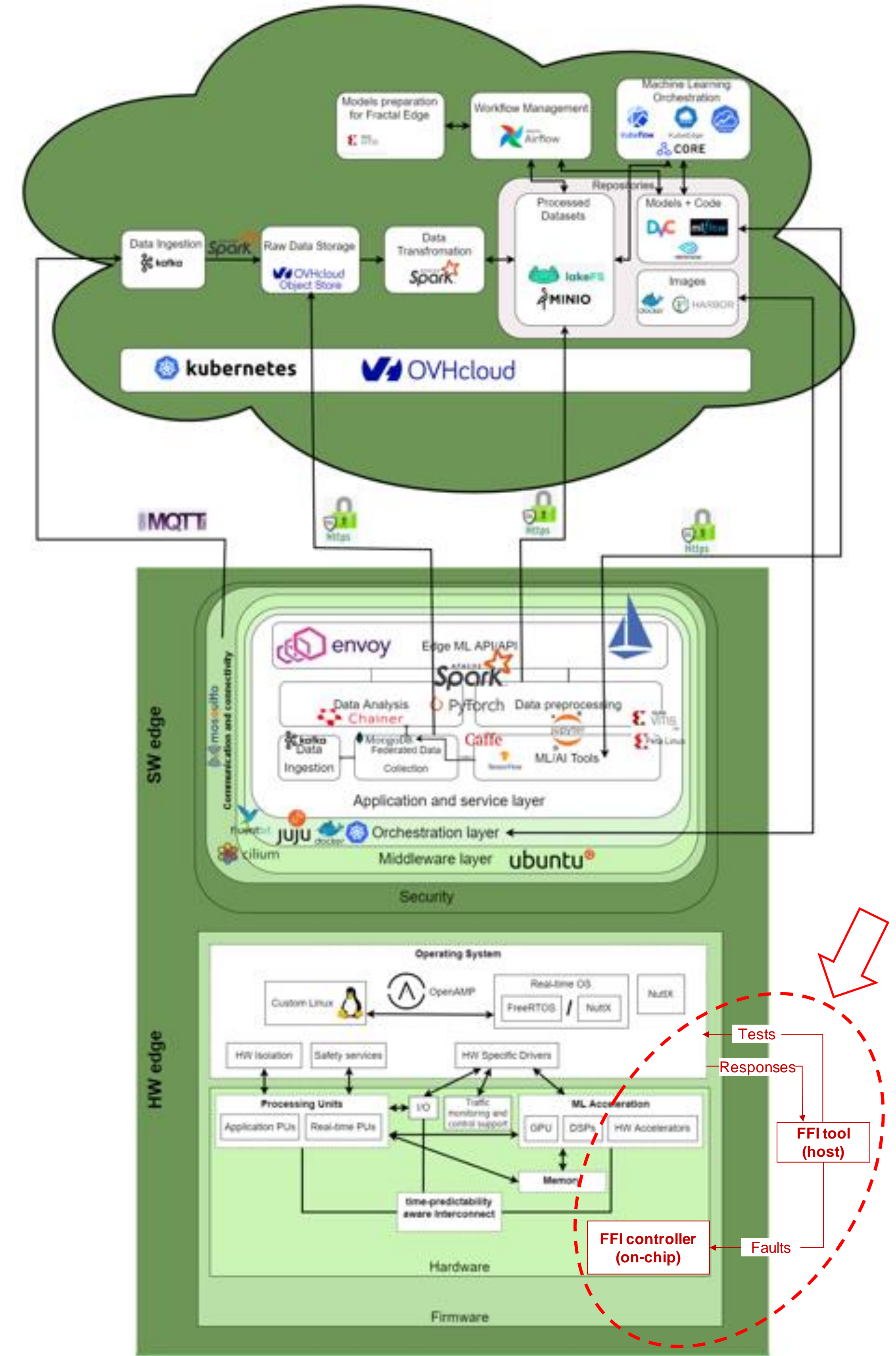
Developed by: UPV



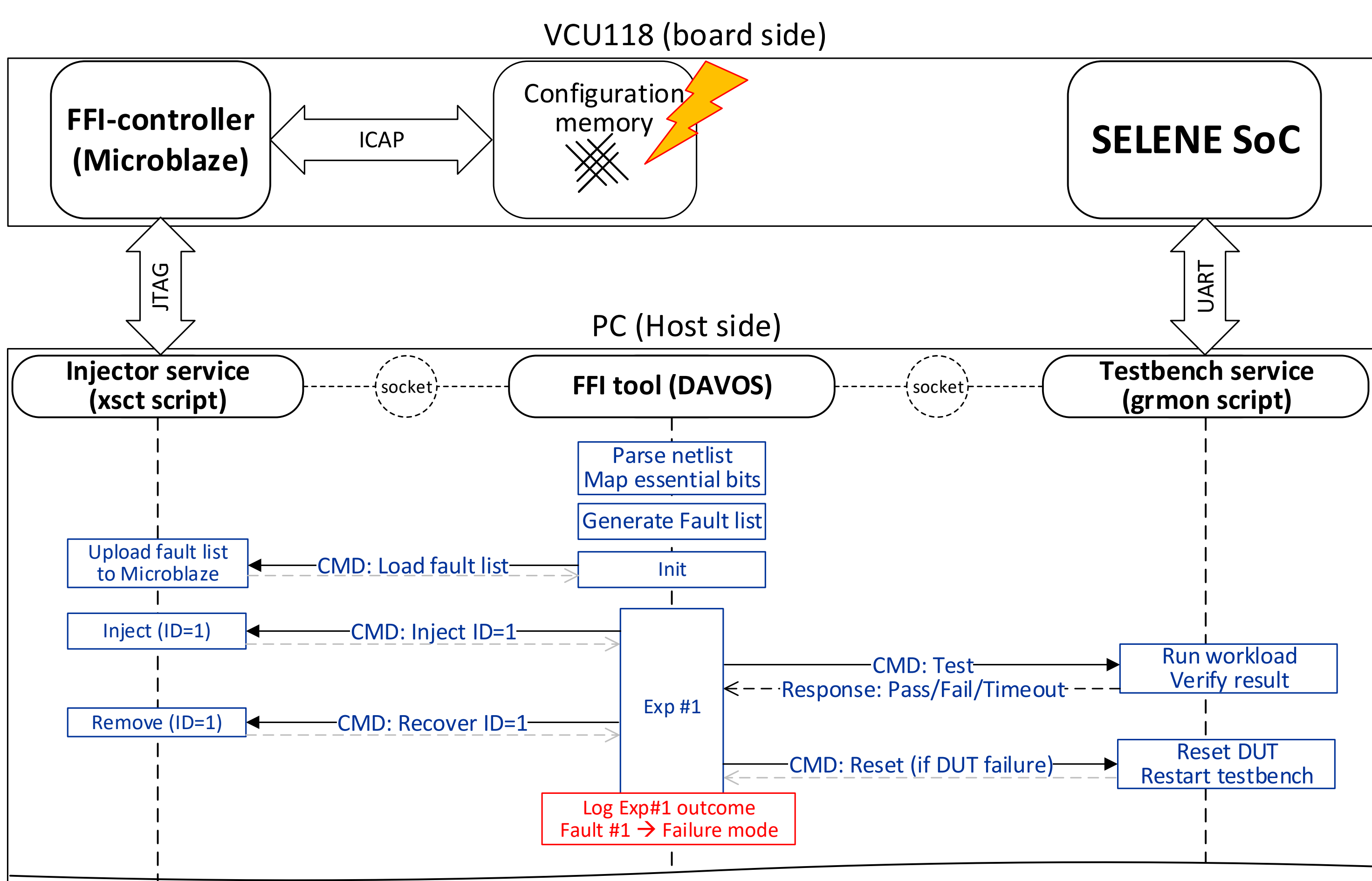
### FFI tool description:

- Objective:**
  - Automated robustness assessment of FPGA prototype against hardware faults
  - Identification of dependability bottlenecks and fault propagation paths
  - Verification of fault-tolerance and dependability-related components (RootVoter, PMU, etc.)
- Fractal features associated:** Safety, Redundancy, Self-monitoring
- Inputs:** FPGA design under test (DUT), workload/testbench, configuration of faultload
- Outputs:** Robustness report describing DUT behavior in presence of faults, rate of observed failure modes for each targeted component, critical/weak points of the DUT
- Integration:** NOEL-V SoC and GRMON debugger (DUT side), DAVOS toolkit (host side)
- Fault injection approach:** Dynamic partial reconfiguration – altering configuration memory (CM) content at runtime, statistical sampling of fault space, essential bits
- Fault models:**
  - Bit-flips in configuration memory – permanent faults in logic and routing (ready to use)
  - Bit-flips in registers and on-chip user memories – transients (ongoing work)

### Component location



### Structure and operation of FFI tool



### Get started

#### 1. Customize FFI configuration (config.xml file):

<FFI	dut_scope	=	"cpu/core0/gpp0/noelv0/cpulooop[2].core/"	Filter fault targets by design hierarchy
	pblock	=	"tiles:X2Y302:X90Y359"	Filter fault targets by FPGA floorplan
	target_logic	=	"LUT"	Filter fault targets by logic type (LUT / BRAM /...)
	sample_size	=	"5000"	Number of sampled fault configurations
	fault_multiplicity	=	"1"	Number of fault targets per configuration
	dut_script	=	"grmon -u -uart /dev/ttyUSB2 -c host_grmon.do" />	Link testbench script to FFI configuration

#### 2. Adapt testbench service to the used workload (SW):

- Customize "host\_grmon.do" for baremetal SW,
- OR define custom testbench with the same interface (commands received via socket):

```

CMD ← SOCKET RECEIVE:
IF CMD=1: Test() {...} → return status: Pass / Failure Mode
IF CMD=2: Reset() {...} → return status: OK
    
```

#### 3. Run fault injection experiment: DAVOS/> python FFI\_tool.py config.xml

```

Injector FFIHostGrmon instantiated from /home2/tuil/DAVOS
Layout loaded for device part: xcvu9p-flga2104-2L-e
Bitstream parsed: /home2/tuil/selene_axi4/selene-hardware/selene-soc/selene-xilinx-vcu118/vivado/noelv-xilinx-vcu118/DavosGenerated/Bitstream.bit
FFI Design Model initialized in 57.1 seconds

Mapped LUTs in dut_scope = "cpu/core0/gpp0/noelv0/cpulooop[2].core/", pblock = None: 48388
Sampled faults: 5000 (population size = 3096832)

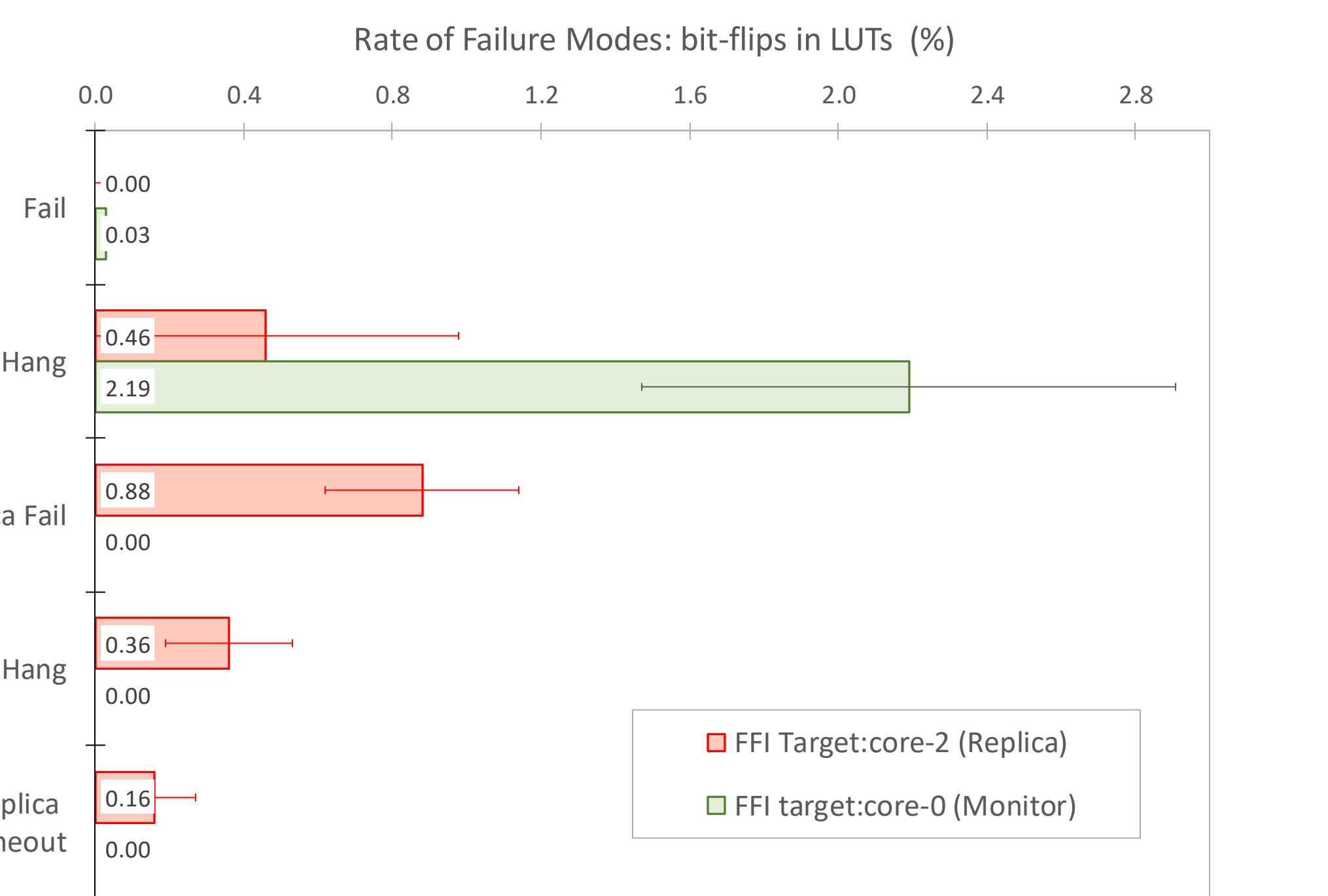
Faultlist loaded: /home2/tuil/selene_axi4/selene-hardware/selene-soc/selene-xilinx-vcu118/vivado/noelv-xilinx-vcu118/DavosGenerated/Faultlist_0.bin

Exp: 3619, Target: cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][0][op1][9]_i_9/bit_02
Injection status : Ok
Injection result : ReplicaFail:f=00000010:t=00000000
Fault removal : Ok
DUT recovery check (post-SEU-remove): Ok
Exp. Time : 0.3 seconds (Total: 2763.8 seconds), Statistics:
Masked: 3549 (98.04% ± 0.45%), Fail: 0 (0.00% ± 0.00%), Hang: 14 (0.39% ± 0.20%),
ReplicaFail: 36 (0.99% ± 0.32%), ReplicaHang: 8 (0.22% ± 0.15%), ReplicaHang: 13 (0.36% ± 0.19%)

Experimental result: Masked: 4996 (98.12% ± 0.38%), Fail: 0 (0.00% ± 0.00%), Hang: 22 (0.44% ± 0.18%),
ReplicaFail: 45 (0.90% ± 0.26%), ReplicaHang: 8 (0.16% ± 0.11%), ReplicaHang: 19 (0.38% ± 0.17%)
FFI summary exported: LOG_2022-06-09_17-53-26.csv
Completed in 4045.1 seconds
    
```

#### 4. Examine logged critical bits (bit-flips that lead to data corruption/timeout/hang failures)

Id	Ce	Mul	FailureMod	Offset	DesignNode	SLR	FAR	Word	Bit	Mask	Time
177	175	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][1][op1][41]_i_5/bit_57	0x00010x00084a08	73	25	0x02000000	0	0
231	229	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/dcojdata[0][S5]_INST_0/bit_26	0x00010x0008aa06	27	10	0x00000000	0	0
392	390	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][1][op2][23]_i_2/bit_22	0x00010x00084102	54	22	0x00000000	0	0
419	417	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[m][result][0][30]_i_8/bit_35	0x00010x00083008	80	23	0x00000000	0	0
422	420	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][1][op1][7]_i_2/bit_57	0x00010x00086408	44	25	0x02000000	0	0
510	508	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][0][op1][0]_i_6/bit_38	0x00010x00085501	59	6	0x00000000	0	0
537	535	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/dcojdata[5][INST_0/bit_59	0x00010x00087e08	42	11	0x00000000	0	0
659	657	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/ramf.rfo/rdata[1][3]_INST_0/bit_12	0x00010x00087907	40	12	0x00001000	0	0
666	664	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][1][op1][1]_i_7/bit_18	0x00010x00087306	25	2	0x00000004	0	0
696	694	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[m][result][1][1]_i_4/bit_35	0x00010x00081c05	53	19	0x00000000	0	0
840	838	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/ff[wdata][1][22]_INST_0/bit_14	0x00010x00086a03	56	14	0x00000400	0	0
873	871	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[e][alu1][1][op1][53]_i_4/bit_29	0x00010x00085d06	86	13	0x00002000	0	0
1056	1054	1	1	1	cpu/core0/gpp0/noelv0/cpulooop[2].core/u0/iu0/syncrregs.r[m][result][1][23]_i_3/bit_34	0x00010x00082801	54	18	0x00004000	0	0



#### 5. Visualize statistical results (rate of observed failure modes)



This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 877056. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Italy, Austria, Germany, Finland, Switzerland.