WP3 Node Architecture & Building Blocks

WP3T32-01: HW Accelerator (SIEFRACC)

Developed by: Siemens AG

Component description

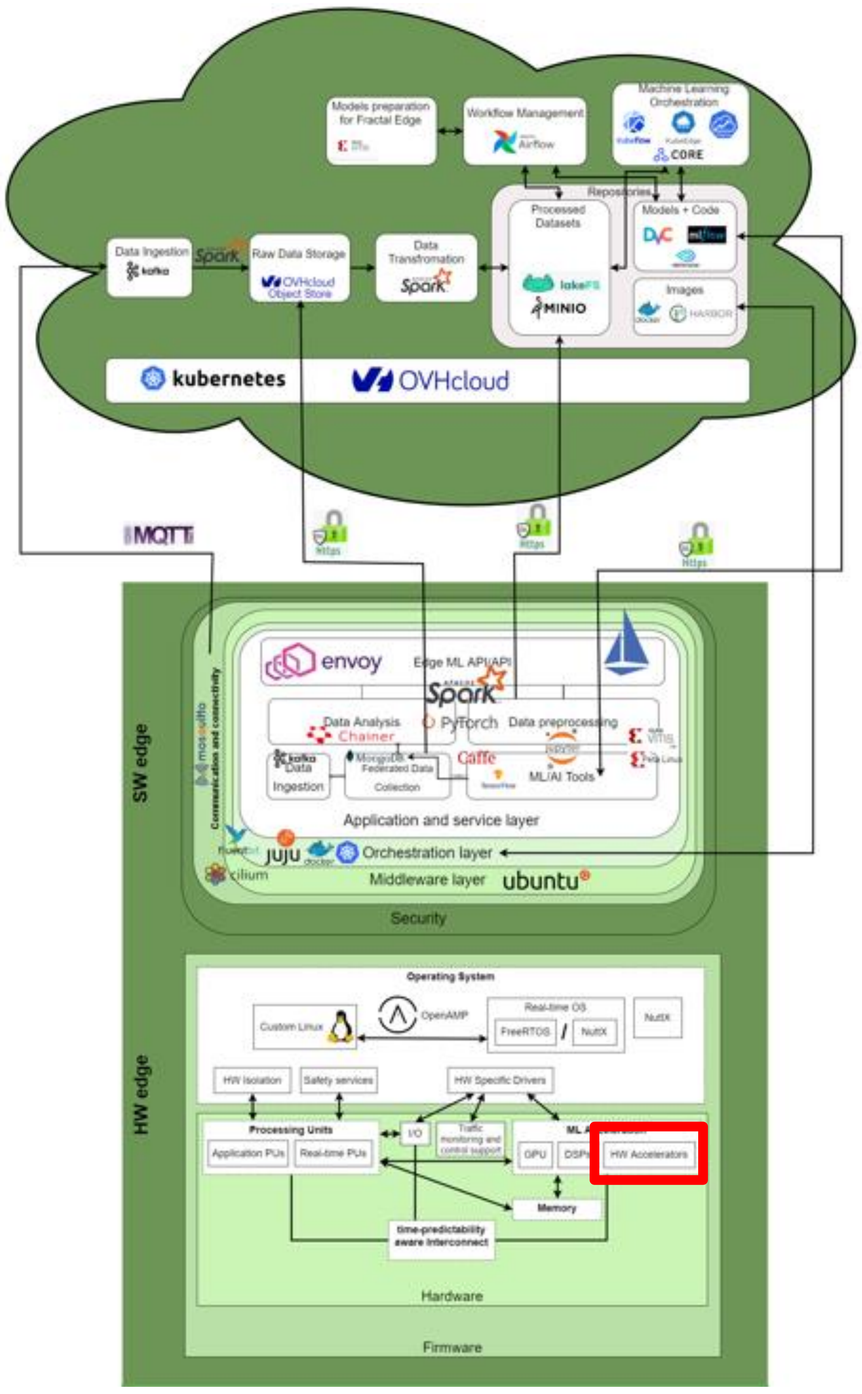
- Objective of the component:
  - Hardware Accelerator (SIEFRACC) is an FPGA solution for accelerating the execution of AI-based algorithms.

- Fractal Features associated:
  - ADAPTABILITY --> AI --> HW --> ML ACCELERATOR

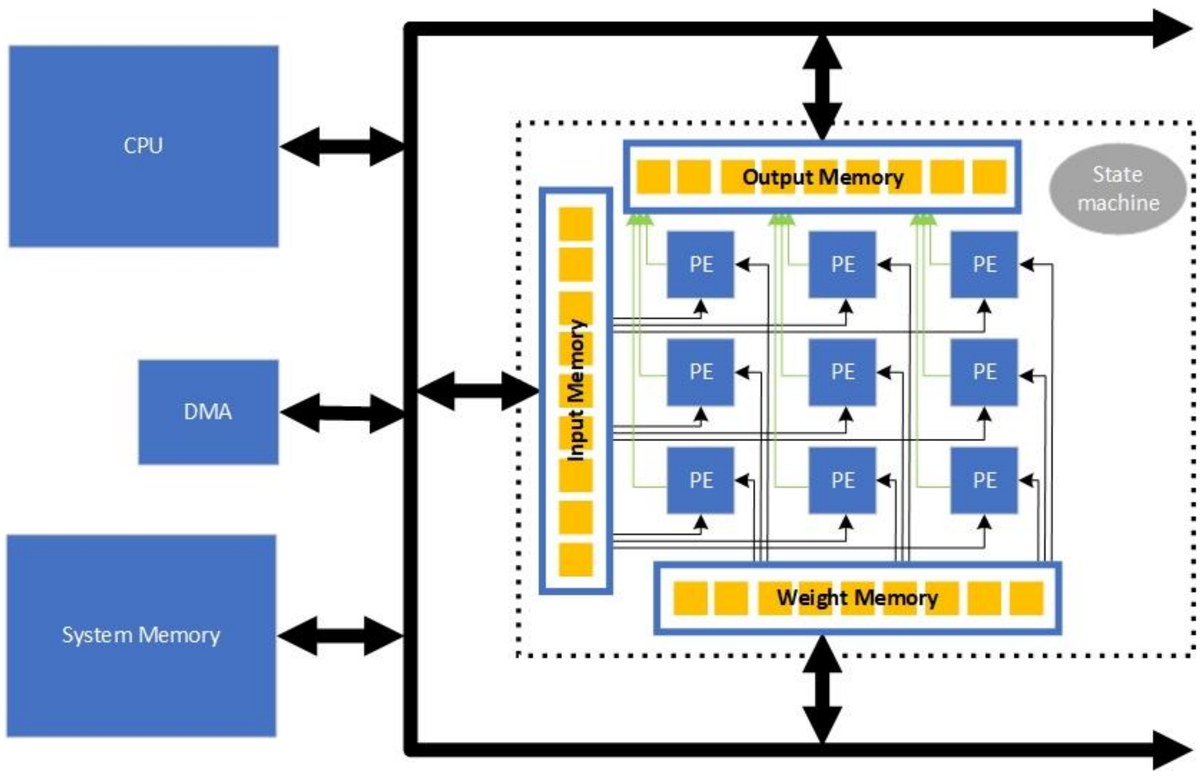
- Inputs/Outputs:
  - INPUT: Input image and weight
  - OUTPUT: Output image

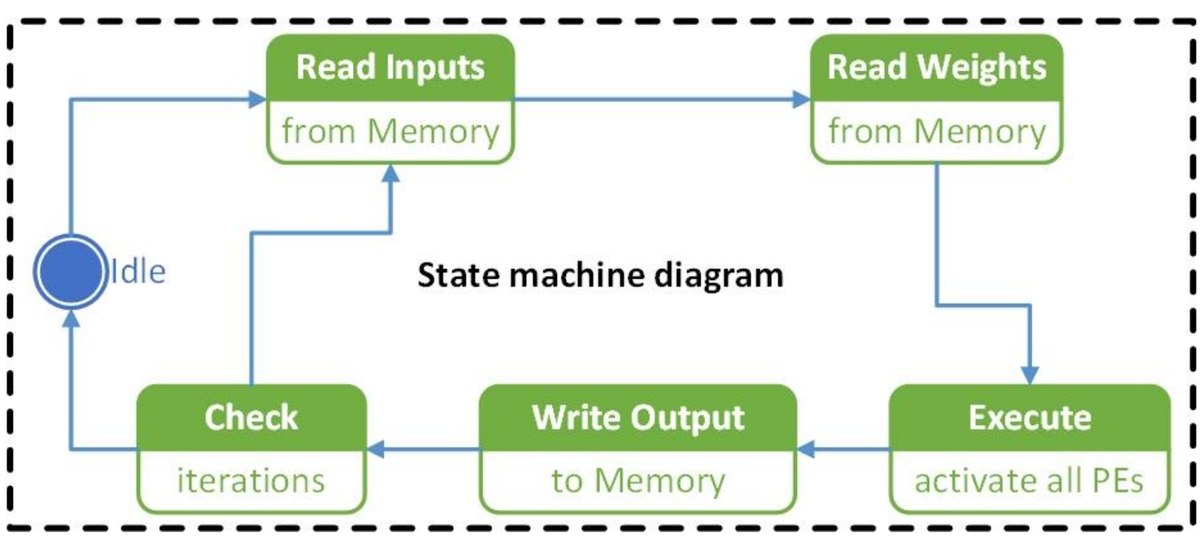
- Integration:
  - CVA64

Component location



Images/Diagrams to describe the component and its processes





Get started

The SIEFRACC hardware accelerator contains a set of nine processing elements (PE) and a local memory. The PEs are organized in a way that each PE performs arithmetic operations in parallel with the other PEs and all of them read/writes the data at the same time directly from/to the local memory. The control of data path is done by the State Machine. It starts by reading the input image, then weights, then performs arithmetic operations and finishes with writing the output to system memory. The accelerator is developed using the Catapult High-Level Synthesis (HLS) toolset and is connected to the CPU through AXI bus.

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