

# WP3 Node Architecture and Building Blocks

## WP3T31-03-UPV-Extensions to the interconnect and other NOEL-V components for Security and Safety

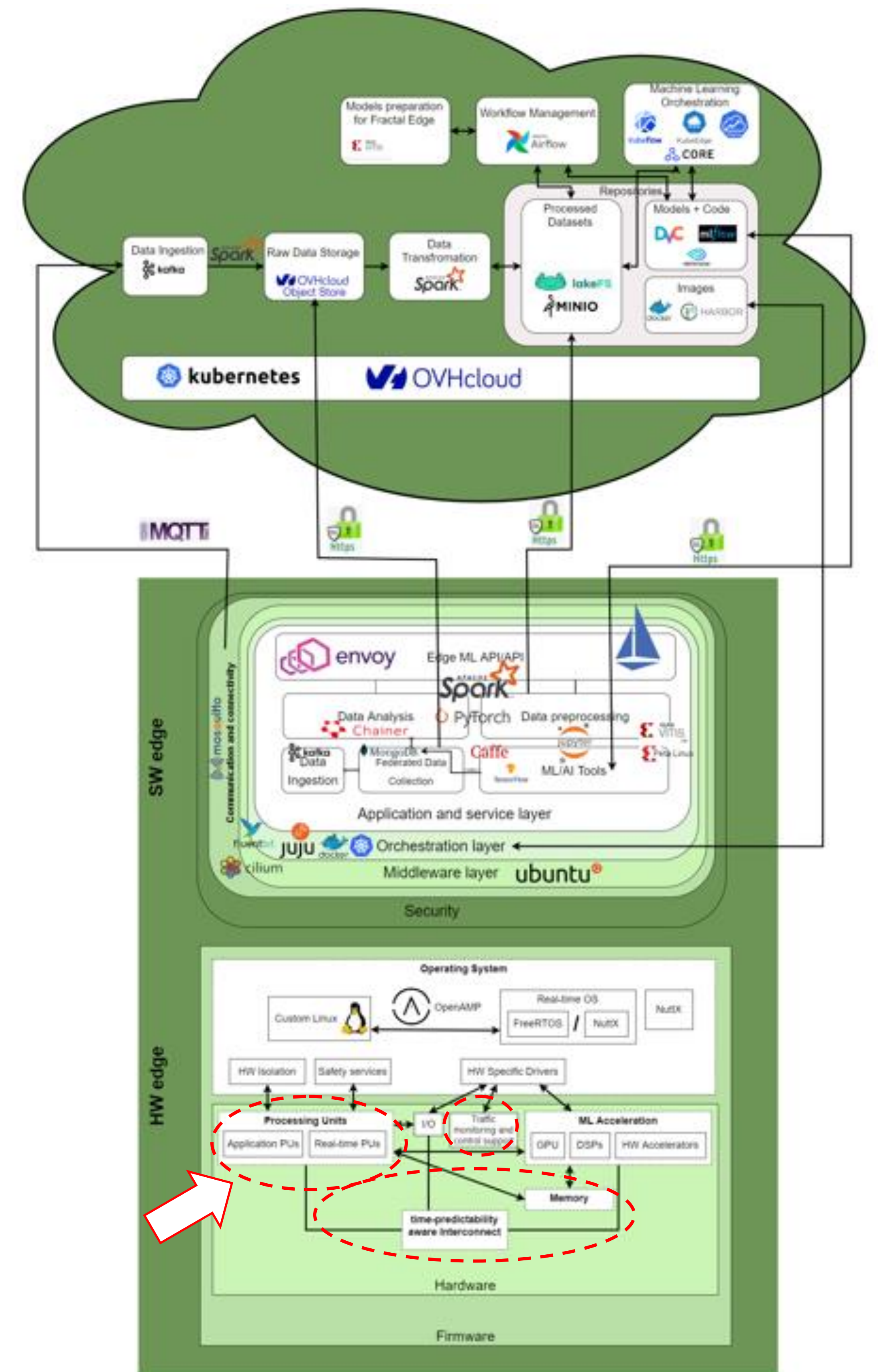
Developed by: UPV



### Hardware support for safety and security description:

- Objective:**
  - ✓ Congestion detection at memory controller for QoS management
  - ✓ Improve real-time predictability
  - ✓ Improve the robustness of NOEL-V system against hardware faults
- Fractal features associated:** Safety, Traffic monitoring, Self-monitoring, Time-predictability
- Integration:** NOEL-V SoC

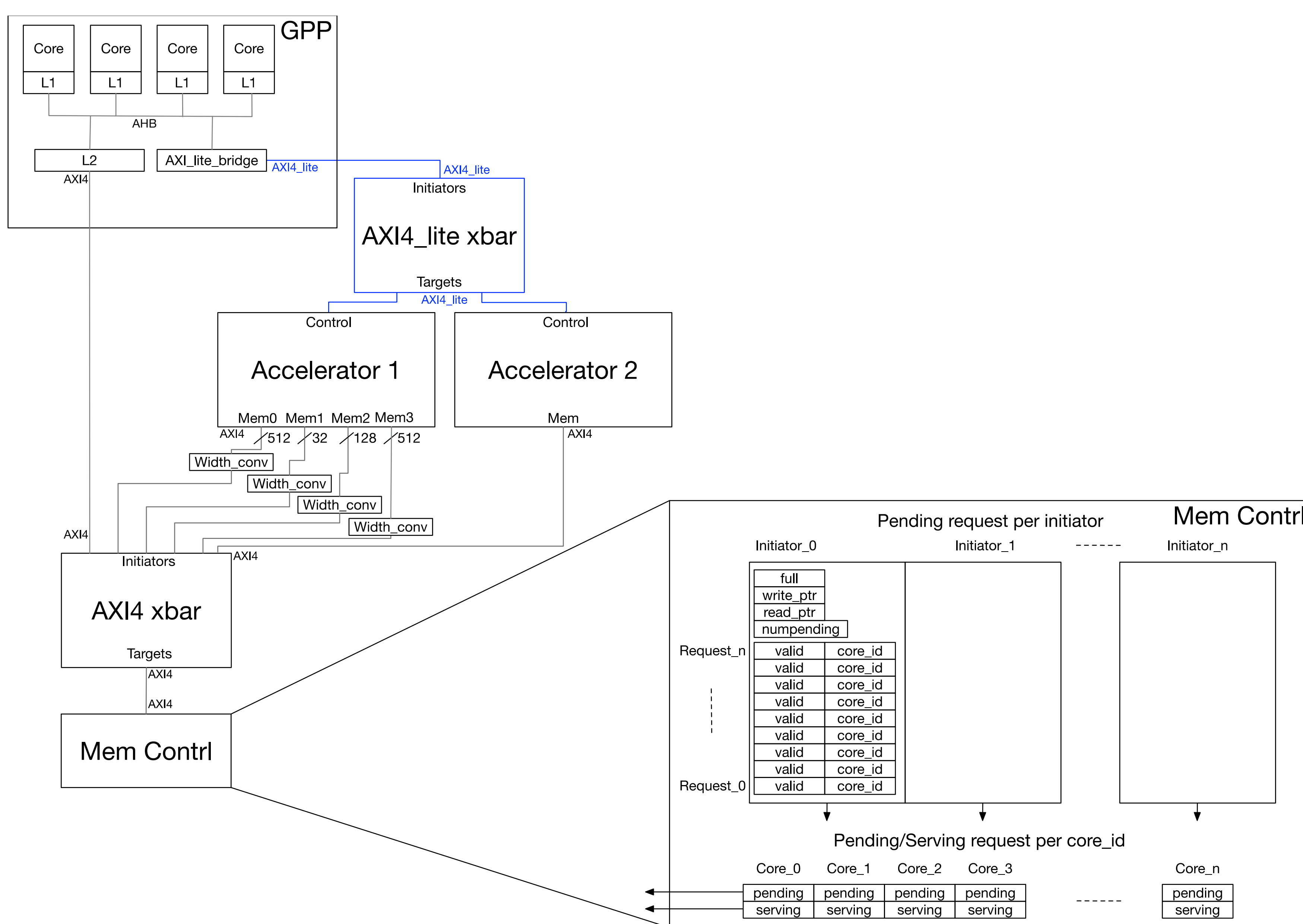
### Component location



### Structure and operation of hardware for safety and security

#### 1. Interconnect and Memory Congestion Monitor

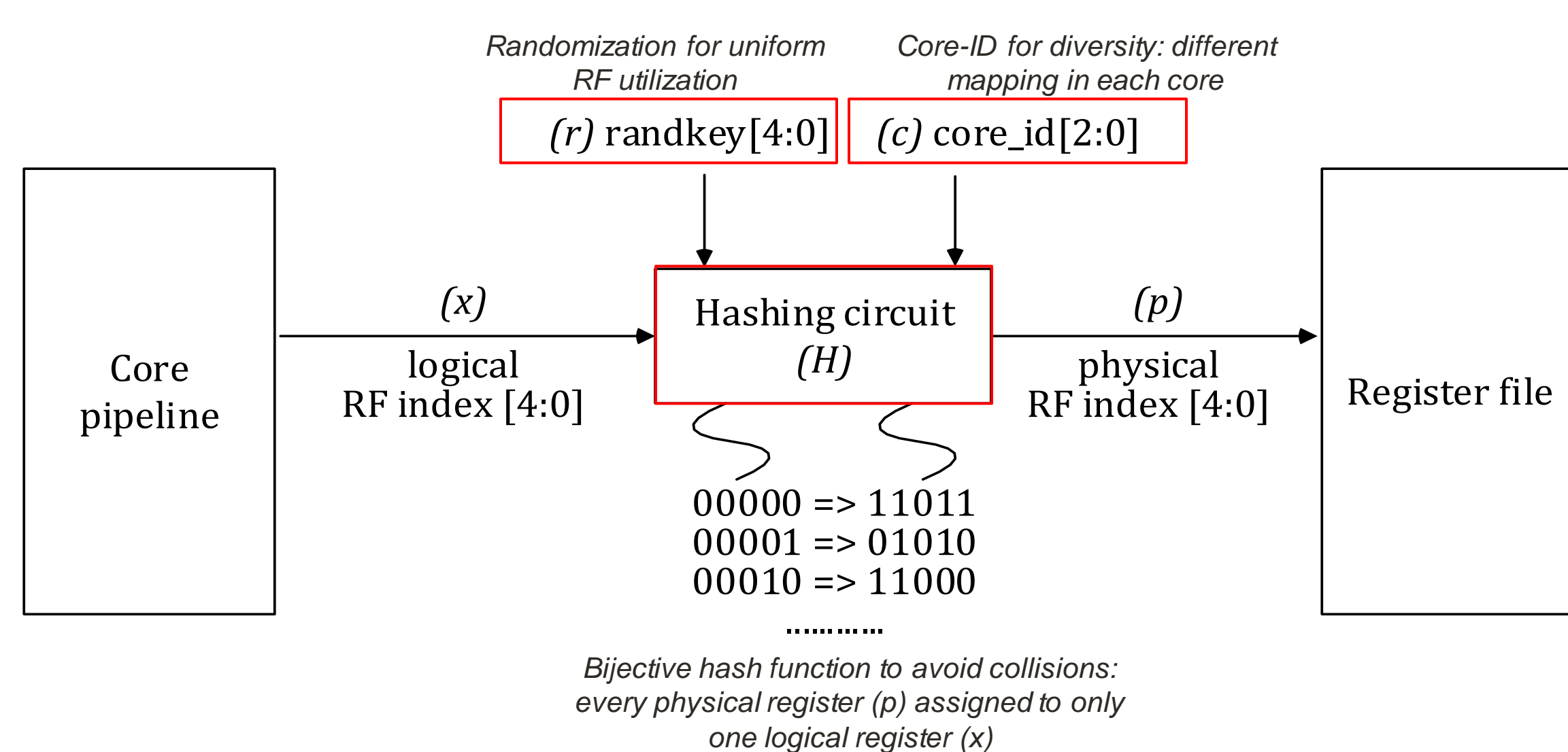
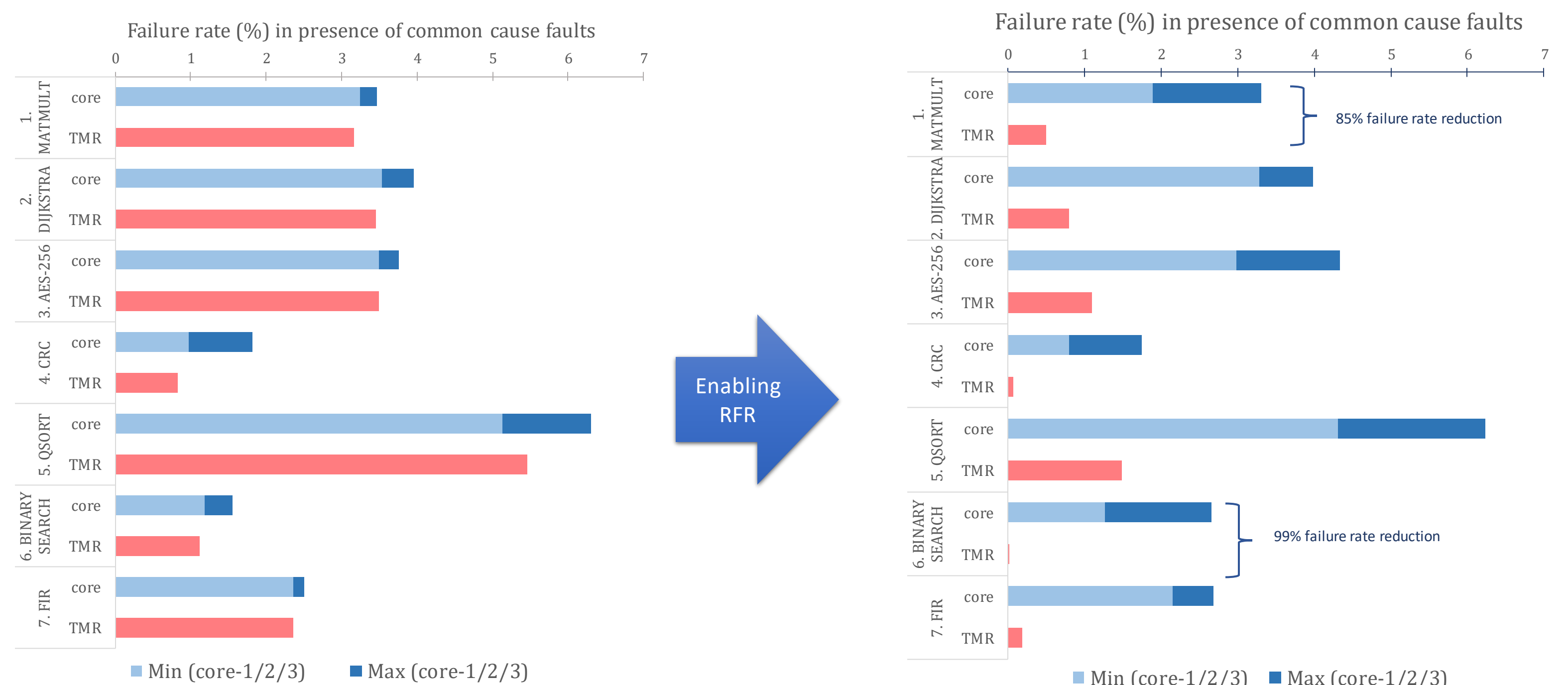
- ✓ Detects the congestion between multiple memory transactions from different sources
- ✓ Master ID propagation through the interconnect
- ✓ Provides congestion signals to other components for QoS management



#### 2. Register File randomization

- ✓ Diversifies mapping between logical and physical registers across processor cores
- ✓ Improves the robustness of RISC-V RF against Common-cause faults by 10x on average
- ✓ Equalizes utilization rate of RF cells → Improves RF lifetime by 4 to 7 times

Efficiency of RFR against common-case faults evaluated by simulation-based fault injection

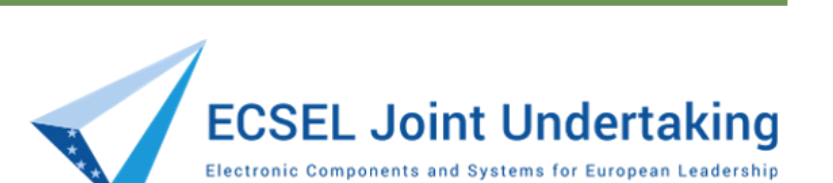


### Get started

This hardware support for safety and security is transparent for the user

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